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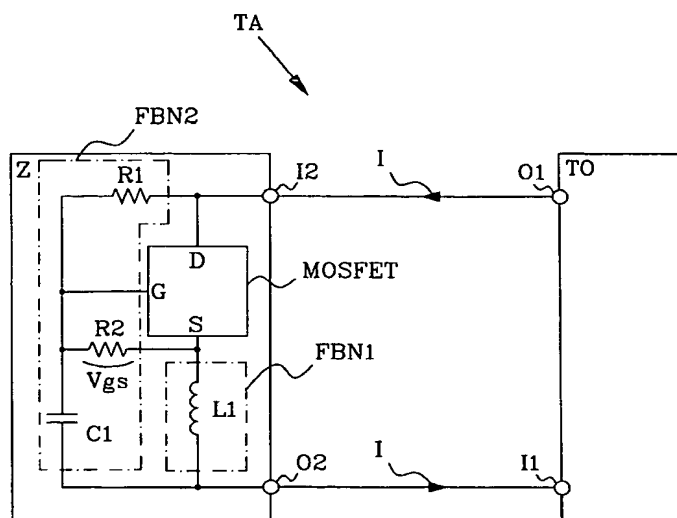
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(54) Title: ACTIVE LOAD ARRANGEMENT



(57) Abstract: The present invention relates to an active load arrangement Z used to provide proper output load to an object TO under test. The arrangement Z comprises a voltage controlled transistor MOSFET having a source S, a gate G and a drain D. The drain D is associated with the gate G and connected to an arrangement input I2 associated with an output O1 of the object under test. The source S is connected to an arrangement output O2 associated with an input I1 of the object under test. A feedback arrangement is connected to the source S and the gate G. The feedback arrangement changes phase and amplitude of the gate-to-source voltage by varying frequency in order to obtain low impedance at low frequencies and high impedance at high frequencies.